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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO
10/749,791	12/29/2003	Jerrold Von Hauck	APPL-P2839 5370 EXAMINER	
28661	7590 08/16/2006			
SIERRA PATENT GROUP, LTD. 1657 Hwy 395, Suite 202			MISIURA, BRIAN THOMAS	
Minden, NV 89423			ART UNIT	PAPER NUMBER
			2112	

DATE MAILED: 08/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

	Applica	ation No.	Applicant(s)				
		10/749,791 HAUCK, JERROLD					
Office Action Summa	ry Examir	ner	Art Unit				
	Brian T	. Misiura	2112				
The MAILING DATE of this cor Period for Reply	nmunication appears on	the cover sheet with the	correspondence address				
A SHORTENED STATUTORY PERIOD WHICHEVER IS LONGER, FROM T  - Extensions of time may be available under the proafter SIX (6) MONTHS from the mailing date of the If NO period for reply is specified above, the maximum of the properties of the propert	HE MAILING DATE OF ovisions of 37 CFR 1.136(a). In no is communication. In much statutory period will apply and or reply will, by statute, cause the anonths after the mailing date of this	THIS COMMUNICATIO event, however, may a reply be ti d will expire SIX (6) MONTHS from application to become ABANDONI	N. Imely filed In the mailing date of this communication. ED (35 U.S.C. § 133).				
Status							
1) Responsive to communication							
2a) This action is <b>FINAL</b> .	·						
,	<del></del>						
closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213.							
Disposition of Claims							
4)⊠ Claim(s) <u>1-10</u> is/are pending in the application.							
4a) Of the above claim(s) is/are withdrawn from consideration.							
5) Claim(s) is/are allowed.							
	Claim(s) 1-10 is/are rejected.						
7) Claim(s) is/are objected 8) Claim(s) are subject to		n requirement					
o) Claim(s) are subject to	estriction and/or election	Troquirement.					
Application Papers							
9)☐ The specification is objected to	•	_					
10)⊠ The drawing(s) filed on <u>29 December 2003</u> is/are: a)⊠ accepted or b)□ objected to by the Examiner.							
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).							
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.							
Priority under 35 U.S.C. § 119							
12) Acknowledgment is made of a ∂ a) All b) Some * c) None		under 35 U.S.C. § 119(a	a)-(d) or (f).				
1. Certified copies of the pr							
2. Certified copies of the priority documents have been received in Application No							
•			ved in this National Stage				
application from the Inte	·		and				
* See the attached detailed Office	e action for a list of the ce	attilled copies not receiv	eu.				
Attachment(s)		A) [] (-tir 2	o. (DTO 412)				
<ol> <li>Notice of References Cited (PTO-892)</li> <li>Notice of Draftsperson's Patent Drawing Re</li> </ol>	view (PTO-948)	4) Interview Summar Paper No(s)/Mail [					
3) Information Disclosure Statement(s) (PTO-1 Paper No(s)/Mail Date		5) Notice of Informal 6) Other:	Patent Application (PTO-152)				

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#### **Detailed Action**

## **Response to Arguments**

Applicant's arguments filed 6/15/2006 have been fully considered but they are not persuasive.

In the applicant's arguments, the applicant states the Masunaga lacks the claimed limitation of "a bus manager sending a configuration packet to all PHYs connected on the bus, the configuration packet containing a minimum gap count parameter value, the minimum gap count parameter value derived from the maximum round trip delay between the first PHY and the second PHY.

The examiner respectfully disagrees with regards to the applicant's arguments. The applicant discloses in claim 1: "calculating a maximum round trip delay between a first PHY and a second PHY connected on the bus by pinging." The examiner points out paragraph [0087] of the applicants specification and figure 9, which states: "the simplest and most accurate Round\_Trip\_Delay determination is afforded when the Bus Manager is one of the leaf nodes in question as shown in Figure 9. Claim 1 as broadly claimed, could be interpreted to include the bus manager as being one of either the 'first PHY' or the 'second PHY' as described in paragraph [0087]. Therefore, with this interpretation of the bus manager of Masunaga being one of the PHY nodes as described by the applicant, Masunaga discloses all the limitations of claim 1.

## Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

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(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

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Claims 1-10 are rejected under 35 U.S.C. 102 (b) as being anticipated by Masunaga et al. U.S. Patent No. 6,909,699.

Per claims 1 and 10, Masunaga discloses: a method of optimizing communication over a high-speed serial bus by minimizing the delay between packets transmitted over the bus, the method comprising:

- calculating a maximum round trip delay between a first PHY and a second PHY connected on the bus by pinging (Masunaga, column 19 lines 30-50, column 20 lines 24-41, figure 40);
- a bus manager sending a configuration packet to all PHYs connected on the bus, the configuration packet containing a minimum gap\_count parameter value, the minimum gap\_count parameter value derived from the maximum round trip delay between the first PHY and the second PHY (column 20 lines 42-47, figure 40)
   (By saying "thereby optimizing the gap count", it is understood that the configuration packet was sent to all nodes.); and
- all PHYs connected on the bus sending packets over the bus using the minimum gap\_count parameter value as delay between packets (column 18 lines 55-65, column 19 lines 1-16) [defines minimum gap-count.], and (column 20 lines 42-47 figure 40).

Per claim 2, Masunaga discloses: the method of claim 1, further comprising preserving an ack/iso gap between packets, wherein a first PHY sent a most recently-sent packet and a second PHY is responding to the first PHY (column 2 lines 40-45, figure 4).

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Per claim 3, Masunaga discloses: the method of claim 2, wherein the second PHY is responding with an ack packet (column 2 lines 40-45, figure 4).

Per claim 4, Masunaga discloses: the method of claim 2, wherein the second PHY is responding with an isochronous arbitration packet (figure 7).

Per claim 5, Masunaga discloses: the method of claim 1, wherein the first PHY sends an isochronous packet, observes a subaction gap, and initiates an arbitration indication (figure 6).

Per claim 6, Masunaga discloses: the method of claim 1, wherein the first PHY sends an asynchronous packet, observes an arbitration reset gap, and initiates an arbitration indication (column 18, lines 34-47, figure 38).

Per claim 6, Masunaga discloses: the method of claim 1, wherein calculating the round trip delay comprises a ping command executed at a link layer level on a node having a first PHY and is directed at a link layer on a node having a second PHY (column 13 lines 7-22 figure 24, and column 19 lines 30-50, column 20 lines 24-41, figure 40).

Per claim 8, Masunaga discloses: the method of claim 7, wherein calculating the round trip delay comprises calculating a round trip delay from a first link on the node having the first PHY and a second link on the node having the second PHY (Masunaga, column 19 lines 30-50, column 20 lines 24-41, figure 40).

Per claim 9, Masunaga discloses: the method of claim 1, wherein the second PHY has a subaction gap timeout value that is greater than the IDLE value that can occur within a subaction and an isochronous interval on the high-speed serial bus (figure 5, sub action gap is smaller than the entire subaction).

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#### Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian T. Misiura whose telephone number is (571) 272-0889. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on (571)272-3676. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Bra Whruno 8/14/2006

SUPERVISORY PATENT EXAMINER